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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,701	02/13/2002	Seon Goo Lee	WK2K1080	1832

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,701	LEE ET AL.	
	Examiner	Art Unit	
	David E Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 27-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Applicant's election of claims 1-19 and 27-31 in the reply filed on 9-27-4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

The information disclosure statement filed 1-17-3 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each foreign patent. It has been placed in the application file, but the foreign patent information referred to therein has not been considered.

The disclosure is objected to because of the following informalities: at page 6, lines 12-14, reference numeral 4 is used to designate different elements, and reference numerals 4 and 5 are used to designate the same element.

Appropriate correction is required.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 8, 9, 12, 14, 17, 19 and 27-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Shin (6798049)

The applied reference has a common assignee and inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

At column 10, line 5 to column 12, line 60, Shin discloses a semiconductor package, comprising: a substrate 10 having a resin 11 layer with first and second surfaces wherein a plurality of electrically conductive patterns 19 are formed thereon, the resin layer having an aperture 16 formed in a central area thereof; a first semiconductor chip 1 having first and second surfaces, the second surface having a plurality of

input/output pads 1a formed thereon, the first semiconductor chip being placed in the aperture of the substrate; a plurality of first conductive wires 20 for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the resin layer; an adhesive 34 attached to the second surface of the first semiconductor chip; a second semiconductor chip 4 having first and second surfaces, the second surface having a plurality of input/output pads 4a formed thereon, the second semiconductor chip being attached to the adhesive; a plurality of second conductive wires 20 for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the resin layer; an encapsulate 31 for encapsulating the aperture the first and second semiconductor chips, and the first and second conductive wires; an inherently conductive and inherently thin film 18 formed on the first surface of the first semiconductor chip, the conductive thin film being extended to the encapsulated portion around the first semiconductor chip and the substrate; wherein the electrically conductive patterns are formed on the first and second surfaces of the resin layer and are connected through at least one conductive via 14; wherein the second semiconductor chip has an inherently insulating layer 34 formed on the first surface thereof.

A semiconductor package, comprising: a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed at a central area thereof; a first semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the first semiconductor chip being placed in the aperture of the substrate; a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the the resin layer; a second semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon; means 34 coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip; a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the resin layer; means 31 for encapsulating the aperture of the substrate, the first and second semiconductor chips, and the first and second conductive wires; a conductive thin film formed on the first surface of the first semiconductor chip, the conductive thin film being extended to the encapsulated portion

around the first semiconductor chip and the substrate; wherein the second semiconductor chip has an insulating layer 34 formed on the first surface thereof.

A semiconductor package, comprising: a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed in a central area thereof; a thin conductive film placed over the aperture and coupled to the electrically conductive patterns on the first surface of the resin layer; a first semiconductor chip having a first surface coupled to the thin conductive film and a second surfaces having a plurality of input/output pads formed thereon; a second semiconductor chip having a first surface coupled to the first semiconductor chip and a second surface having a plurality of input/output pads formed thereon; an encapsulate for encapsulating the aperture and the first and second semiconductor chips; a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer; a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the second surface of the resin

layer; an adhesive attached to the second surface of the first semiconductor chip; a plurality of conductive balls 40 coupled to the electrically conductive patterns formed on the second surface of the resin layer.

To further clarify, the film is inherently conductive because it is comprised of matter, and matter inherently conducts physical forces and electromagnetic, thermal and sound energy. Also, the film is inherently thin because it is, by definition, a thin covering or coating.

To further clarify, the layer 14 is inherently insulating because it insulates the first and second chip from direct contact, and because it is comprised of matter, and matter is inherently to some degree insulating to electromagnetic, thermal and sound energy.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the

time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-9, 12-17, 19 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinsman (6172419) and Fukui (6657290).

At column 3, lines 41-56; column 4, line 19 to column 6, line 5; and column 6, lines 51-56, Kinsman discloses the following:

A semiconductor package, comprising: a substrate having a resin 102 layer with first and second surfaces wherein a plurality of electrically conductive patterns 110, 112 are formed thereon, the resin layer having an aperture 114 formed in a central area thereof; a first semiconductor chip 120 having first and second surfaces, the second surface having a plurality of input/output pads 122 formed thereon, the first semiconductor chip being placed in the aperture of the substrate; a plurality of first conductive wires 124 for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the resin layer; an adhesive

126 attached to the second surface of the first semiconductor chip; an encapsulate 126 for encapsulating the aperture, the first semiconductor chip, and the first conductive wires; a conductive thin film 116 formed on the first surface of the first semiconductor chip, the conductive thin film being extended to the encapsulated portion around the first semiconductor chip and the substrate; wherein the electrically conductive patterns are formed on the first and second surfaces of the resin layer and are connected through at least one conductive via 108.

A semiconductor package, comprising: a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed at a central area thereof; a first semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the first semiconductor chip being placed in the aperture of the substrate; a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the the resin layer; means 126 for encapsulating the aperture of the substrate, the first semiconductor chip, and the first conductive wires; a conductive thin film formed on the first

surface of the first semiconductor chip, the conductive thin film being extended to the encapsulated portion around the first semiconductor chip and the substrate.

A substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed in a central area thereof; a thin conductive film 126 placed over the aperture and at least physically coupled to the electrically conductive patterns on the first surface of the resin layer; a first semiconductor chip having a first surface coupled to the thin conductive film and a second surfaces having a plurality of input/output pads formed thereon; an encapsulate for encapsulating the aperture and the first and second semiconductor chips; a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns 110 formed on the second surface of the resin layer; an adhesive attached to the second surface of the first semiconductor chip; a plurality of conductive balls 228 at least indirectly physically coupled to the electrically conductive patterns formed on the second surface of the resin layer.

However, Kinsman does not appear to explicitly disclose a second semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the second semiconductor chip being attached to the adhesive; a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the resin layer; an encapsulate for encapsulating the second semiconductor chip, and the first and second conductive wires; wherein each of first conductive wires are stand off stitch bonded; wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip; wherein a conductive ball is coupled to the input/output pad of the first semiconductor chip and the first conductive wire is stitch-bonded to the conductive ball; wherein each of the plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns on the resin layer of the substrate are normal wire bonded; wherein one end of each second conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the

second semiconductor chip; wherein a conductive ball is fused to the input/output pad of the second semiconductor chip and the second conductive wire is stitch-bonded to the conductive ball; wherein the second semiconductor chip has an insulating layer formed on the first surface thereof; wherein the horizontal width of the second semiconductor chip is wider than that of the first semiconductor chip; means coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip; means for encapsulating the second semiconductor chip, and the second conductive wires; wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip so that the a curved portion of the first conductive wire is placed on the electrically conductive pattern; wherein one end of each second conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the second semiconductor chip so that a curved portion of the second conductive wire is placed on the electrically conductive pattern.

Nonetheless, at column 1, lines 15-22; column 2, lines 21-31; column 3, lines 46-48; column 4, lines 54-57; column 5, line 51 to column 6, line 34; column 8, lines 51-64; column 9, line 44 to column 11, line 7; column 11, lines 21-26; column 12, lines 19-46; column 14, lines 2-14 and 33-53; and column 15, lines 14-17, Fukui discloses a second semiconductor chip 31 having first and second surfaces, the second surface having a plurality of input/output pads 21 formed thereon, the second semiconductor chip being attached to the adhesive 6; a plurality of second conductive wires 3 for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns "wire bonding terminal" formed on the resin layer 7; an encapsulate 15 for encapsulating the second semiconductor chip, and the first and second conductive wires; wherein each of first conductive wires are stand off stitch bonded "reverse wire bonding"; wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip "reverse wire bonding"; wherein a conductive ball is coupled to the input/output pad of the first semiconductor chip and the first conductive wire is stitch-bonded to the conductive ball "reverse wire bonding"; wherein one end of each second

conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the second semiconductor chip; wherein a conductive ball is fused to the input/output pad of the second semiconductor chip and the second conductive wire is stitch-bonded to the conductive ball; wherein the second semiconductor chip has an insulating layer 5 formed on the first surface thereof; wherein the horizontal width of the second semiconductor chip is wider than that of the first semiconductor chip; means 5, 6 coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip; means 15 for encapsulating the second semiconductor chip, and the second conductive wires; wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip so that the a curved portion of the first conductive wire is placed on the electrically conductive pattern; wherein one end of each second conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the second semiconductor chip so that a curved portion of the second conductive wire is placed on the electrically

conductive pattern. Moreover, it would have been obvious to combine this disclosure of Fukui with the disclosure of Kinsman because, as disclosed by Fukui as cited, it would improve the performance of the semiconductor package by providing a plurality of chips and it would desirably facilitate manufacture of a package having small outer dimensions.

Also, neither Kinsman nor Fukui disclose a single embodiment wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip and each of the plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns on the resin layer of the substrate are normal wire bonded.

Nevertheless, as cited Fukui discloses an embodiment wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip, and an embodiment wherein each of the plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns on the resin layer of the substrate are normal wire

bonded "forward wire bonding." In addition, it would have been obvious to substitute the reverse wire bonding of the first semiconductor chip of one embodiment for the forward wire bonding of the embodiment wherein both the first and second chip are forward bonded because it would reduce package thickness. In any case, it would have been obvious to substitute the wire bonding of one embodiment for at least some of the wire bonding of the other embodiment because it would provide wire bonding, and substitution of a known element based on its suitability for its intended use has been held to be prima facie obvious. See MPEP 2144.07.

Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinsman and Fukui as applied to claims 9 and 17, and further in combination with Jones (5639695).

Kinsman and Fukui do not appear to explicitly disclose wherein the electrically conductive patterns formed on the second surface of the resin layer are electrically connected to the conductive thin film.

Notwithstanding, at column 1, lines 12-17; and column 5, line 46 to column 6, line 13, Jones discloses wherein the electrically conductive patterns 109 formed on the second surface of the resin layer are electrically connected to the conductive thin film 98. Furthermore, it would have been

obvious to combine the electrical connection of Jones with the disclosure of the applied prior art because it would facilitate use of the conductive thin film of Kinsman and Fukui as a ground plane.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kinsman and Fukui as applied to claim 1, and further in combination with Lo (6555902).

Kinsman and Fukui do not appear to explicitly disclose wherein the adhesive is silicon having an adhesive layer formed on a top and bottom surface thereon.

Regardless, at column 1, lines 36-40; column 3, lines 26-31; column 4, lines 1-42, Lo discloses wherein the adhesive is silicon 420 having an adhesive layer 404 formed on a top and bottom surface thereon. In addition, it would have been obvious to substitute the adhesive of Lo for the adhesive of the applied prior art because it would have a desirable coefficient of expansion and it would minimize stress. Also, it would have been obvious to substitute the adhesive of Lo for the adhesive of the applied prior art because it would provide an adhesive, and substitution of a known element based on its suitability for its intended use has been held to be prima facie obvious. See MPEP 2144.07. Further, it would have been

obvious to substitute the adhesive of Lo for the adhesive of the applied prior art because it would provide an alternative adhesive when the use of the adhesive of the applied prior art becomes infeasible, e.g., when the adhesive of the applied prior art is cost ineffective or unavailable. Still further, it would have been obvious to combine the adhesive of Lo with the adhesive of the applied prior art because it would provide an adhesive. Indeed, it has been held that it is obvious to combine two processes for the same purpose. In re Novak 16 USPQ2d 2043. Similarly, "It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose . . . . [T]he idea of combining them flows logically from their having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 205 USPQ 1069, 1072 (CCPA 1980) (citations omitted) (Claims to a process of preparing a spray - dried detergent by mixing together two conventional spray - dried detergents were held to be prima facie obvious.). See also, In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960) (Claims directed to a method and material for treating cast iron using a mixture comprising calcium carbide and magnesium oxide were held unpatentable over prior art disclosures that the aforementioned components

individually promote the formation of a nodular structure in cast iron.); and Ex parte Quadranti 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992) (Mixture of two known herbicides held prima facie obvious).

Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinsman (6172419) and Lo (6555902).

As cited supra, Kinsman discloses a semiconductor package, comprising: a substrate having a resin 102 layer with first and second surfaces wherein a plurality of electrically conductive patterns 110, 112 are formed thereon, the resin layer having an aperture 114 formed in a central area thereof; a first semiconductor chip 120 having first and second surfaces, the second surface having a plurality of input/output pads 122 formed thereon, the first, semiconductor chip being placed in the aperture of the substrate; a plurality of first conductive wires 124 for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the resin layer; an adhesive 126 attached to the second surface of the first semiconductor chip; an encapsulate 126 for encapsulating the aperture, the first semiconductor chip, and the first conductive wires.

However, Kinsman does not appear to explicitly disclose a second semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the second semiconductor chip being attached to the adhesive; a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the resin layer; an encapsulate for encapsulating the second semiconductor chip, and the second conductive wires.

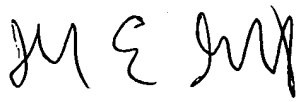
Nonetheless, as cited supra, Lo discloses a second semiconductor chip 409 having first and second surfaces, the second surface having a plurality of input/output pads 422 formed thereon, the second semiconductor chip being attached to the adhesive 404, 420; a plurality of second conductive wires 410b for connecting the input/output pads of the second semiconductor chip to the layer 402; an encapsulate 414 for encapsulating the second semiconductor chip, and the second conductive wires. Furthermore, it would have been obvious to combine this disclosure with the disclosure of Kinsman because, as taught by Lo, it would desirably increase the package capacity and density.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

For information on the status of this application applicant should check PAIR: Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (703) 872-9306.



David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
8-Dec-04